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Thermodynamics limits in Oscillators and Phase Locked Loops

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Thermodynamics limits in Oscillators and Phase Locked Loops

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***Abstract*—In this paper the impact of thermal noise in time domain signal processing is reviewed with an emphasis on oscillators and phase locked loops. It will be shown that both oscillators and phase-locked loops display an upper bound in their efficiency that is fundamentally thermodynamic limited. Such upper bound will be used to derive two comparative figure-of-merits (FoMs) that resemble the one already present in literature. Finally, an analysis of the state of the art of the designs already present in literature confirms the proposed analysis.**

***Index Terms*—figure of merit (FOM), phase-locked loop (PLL), phase noise, signal to noise ratio (SNR), voltage-controlled oscillator (VCO), jitter, absolute jitter, time-domain**

I. Introduction

The most common time-domain circuits in electronics are oscillators and phase locked loop (PLL) where the information is contained in a time difference between two events rather than the voltage drop between two terminals. Recently it has been shown that both time and voltage domain circuits are ultimately thermodynamically limited in a similar way, which leads to a straightforward relationship between power dissipation and signal to noise ratio (SNR) achievable [1]. In this paper, after an overview of the thermodynamic limits for time-domain circuits, it will be demonstrated that such fundamental limit is also behind the most common benchmarking figure-of-merits used for oscillators and PLLs. The presented derivation will allow to identify also thermodynamic upper bounds for such FOMs and intrinsic limitations when used in the attempt to provide a fair comparison between different designs.

The paper is structured as follows: in Section II an overview of the thermodynamic limit in time-domain signal processing is presented. In section III, thermodynamic limits of Oscillators and PLL are discussed. A relationship between the oscillator and PLL FOMs is derived in Session IV which is accompanied with a discussion about the restrictions in the use of such FOMs. Paper ends by introducing a new FoM to benchmark the architecture efficiency of the PLLs regardless of the oscillator and reference frequency adopted.

II. Thermodynamic Limit in Time-Domain Signal Processing

In voltage domain, the maximum and the minimum signals that can be processed are limited by the voltage supply and the thermal noise respectively. These boundaries define the signal-to-noise ratio (SNR) of the circuit and consequently its performance [1]. In time-domain, the jitter noise sets a lower bound in the time difference detectable, while the upper bound is set by the maximum delay generated by the circuit.

In the case of an inverter, the relationship between power (P) and the SNR achievable when used as an integrator has been evaluated by Enz et.al. in [2] as follows:

$$Power = 8\mathrm{kT}f_{BW}SNR = 4\mathrm{kT}f_{BW}SNR\alpha_V \tag{1}$$

where k is the Boltzmann constant and T is the temperature of the circuit f_{BW} is the bandwidth of the circuit and α_V a coefficient set to 2 and f is the bandwidth of the system. When the inverter is used as a delay stage, the jitter noise produced by the inverter and the maximum delay achievable can be used to achieve an expression of power versus SNR.

The expression of the jitter added by a CMOS inverter as a function of the generated delay was evaluated by Abidi in [6] and is given by

$$\sigma^2 = \frac{8\gamma kT{t_d}^2}{CV_{DD}(V_{DD}-V_t)} + \frac{4kT{t_d}^2}{CV_{DD}{}^2} \tag{2}$$

where σ is the jitter, t_d the delay of the inverter, γ the thermal noise coefficient for the transistor, V_t is the transistor voltage threshold. Equation (2) can be used for both transitions (i.e. form V_{DD} to 0 and vice versa) [6]. Starting from (2) it is possible to define the SNR of the inverter working as a delay stage as

$$SNR = \frac{{t_d}^2}{\sigma^2} = \frac{1}{\frac{8\gamma kT}{CV_{DD}(V_{DD}-V_t)} + \frac{4kT}{CV_{DD}{}^2}} \tag{3}$$

Notice that, the SNR of the inverter in time domain is independent of the delay generated, being a function of the capacitive load C, the voltage supply and the transistor threshold. For an easier comparison with (1), (3) can be rewritten as

$$SNR = \frac{C}{4kT\alpha_T}{V_{DD}}^2 \tag{4}$$

with

$$\alpha_T = \frac{2\gamma V_{DD}}{V_{DD}-V_t} + 1 \tag{5}$$

Equation (4) looks very like (1) except for the factor α_T. In fact, while in voltage domain $\alpha_V = 2$, in time domain α_T is technology dependent because it is a function of the ratio between the voltage threshold and the voltage supply. Since the power consumption of the stage in both cases is the same, the following relationship between power and SNR in time domain results:

$$Power = 4\text{kT}f_{BW}SNR\alpha_T \quad (6)$$

III. VCO AND PLL THERMODYNAMIC FOMS

From (6) it is possible to define an upper limit for SNRf_{BW}/P given by 4kTα_T, which limits efficiency in time-domain signal processing (without resonators). The relationship between the SNR achievable by a circuit for a given power dissipation P and bandwidth BW can be expressed by

$$\frac{P}{SNR \cdot f_{BW}} = 4kT\alpha \quad (7)$$

Since in voltage domain the relationship between SNR, f_{BW} and P is constant and thermodynamically limited to 8kT, (7) has been used as basis in the definition of several FOMs which in the most trivial expression is given by

$$FOM = \frac{SNR \cdot f_{BW}}{P} \quad (8)$$

Since in time domain circuits SNR can be defined as

$$SNR = \frac{(\Delta t)^2}{\sigma_a^2} \quad (9)$$

where σ_a is, the jitter accumulated over the time Δt [1], by choosing $f_{BW} = 1/\Delta t$, (8) can be rewritten as

$$FOM = \frac{\Delta t}{P.\sigma_a^2} \quad (10)$$

and can be used to benchmark oscillators and PLL from the point of view of the thermodynamic limit previously highlighted.

A. Oscillator FOM

In literature, the most common FOM used to characterize an electrical oscillator is given by

$$FOM_{osc} = \frac{{f_o}^2}{\Delta f^2.\mathcal{L}(\Delta f)} . \frac{1}{P} \quad (11)$$

Where f_o is the oscillation frequency, Δf is the frequency offset from f_o, $\mathcal{L}(\Delta f)$ is the phase noise spectral density evaluated at an offset Δf and P is the power dissipated (usually normalized to 1mW). Although historically (11) has been derived by a simple rearrangement of the empirical Leesons' model of the phase noise in an oscillator [4], it will be shown that (11) can be derived by starting from (10).

Since in a free running VCO, the jitter square accumulated in N clock cycles is ideally N times the jitter square accumulated in one cycle[1], by setting $\Delta t = NT_o$ gives $\sigma_a^2 = N{\sigma_p}^2$, where $T_o = 1/f_o$ is the oscillation period and σ_p is the period jitter. Substituting Δt with NT_o, and σ_a^2 with $N{\sigma_p}^2$ in (10) leads to the following

$$FOM_{osc} = \frac{NT_o}{N{\sigma_p}^2.P} = \frac{1}{f_o \cdot {\sigma_p}^2 \cdot P} \quad (12)$$

Based on [6], the period jitter, σ_p, can be expressed in term of phase noise, $\mathcal{L}(\Delta f)$, as follows

$${\sigma_p}^2 = \mathcal{L}(\Delta f) \cdot \frac{\Delta f^2}{{f_o}^3} \quad (13)$$

By substituting (13) in (12) the traditional FOM_{osc} for the oscillator expressed by (11) is obtained.

Since the proposed derivation started from (8), an upper bound for its value is expected, as found for filters, amplifier and analog-to-digital converters. However, it should be noted that the limits imposed by (8) is intended for circuits where no resonances are present. In presence of a resonance such limits can be overcome as demonstrated in the analysis proposed in [7].

B. PLL FoM

In the case of PLLs, a very straightforward FOM, which relates the total integrated jitter accumulated, σ_a, and the overall power consumption, P, was derived by Gao at al. [4]. Such FOM is expressed as

$$FOM_{PLL,dB} = -10Log\left(\left(\frac{1s}{\sigma_a}\right)^2 \cdot \frac{1}{P}\right) \quad (14)$$

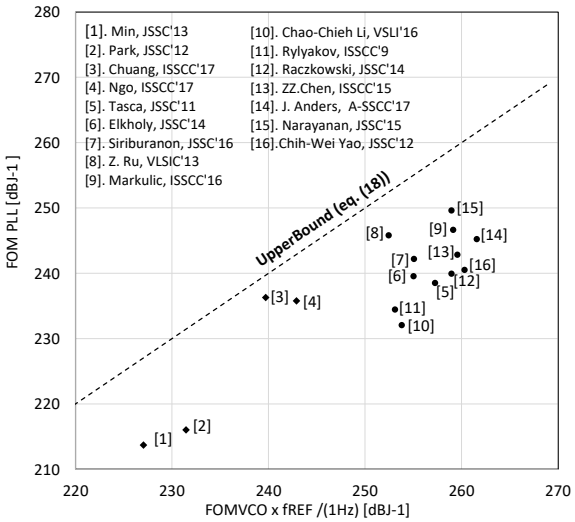
where P is the PLL power normalize to 1mW. The above FOM_{PLL} was derived empirically through a detailed analysis on the relationship between phase noise and power consumption for the different building blocks constituting a generic PLL [4]. However, in this paper we will demonstrate that also such FOM is also a rearrangement of (10). Therefore, it is more general than what its original derivation could suggest.

As mentioned, for a free running oscillator, the jitter square accumulated in N clock periods is N times the period jitter square. Hence, the oscillators' FOM derived by using (10) became independent of integration-time of the jitter (i.e. Δt). However, this is not the case for PLLs because the oscillator is locked, since its phase noise is actively suppressed within the PLL bandwidth. Because of this, unlike a standalone VCO, PLL's integrated jitter does not diverge to infinity if assumed locked to an ideal jitter-free reference. This means that ideally the SNR expressed by (9) improves as Δt increases. Hence, for a fair comparison between different designs, a reference integration time Δt should be defined in such a way that allows for the phase noise suppression within the bandwidth of PLL to be considered. For example, setting Δt = 1s and substituting it into (10) leads to the following expression for the PLL FoM

$$FOM_{PLL} = \frac{\Delta t}{P.\sigma_a^2} = \frac{1s}{\sigma_a^2.P} \quad (15)$$

where σ_a^2 is the jitter integrated from $f = 1Hz$ to $f = \infty$, which for a PLL converges to the jitter integrated over the whole frequency range. It should be noted that this expression is very similar to the one introduced by Gao in a logarithmic form (i.e. (14)). Equation (15) differs from (14) in two aspects: first, it is inversely proportional to jitter and power so that a larger number corresponds to a lower power consumption, and jitter. Second, in the proposed derivation the unit of the FOM is J^{-1} (or dBJ^{-1} in a logarithmic form) as for (11) and (8) (when power is not to normalized to 1mW).

[1] This is true if only thermal noise is considered.



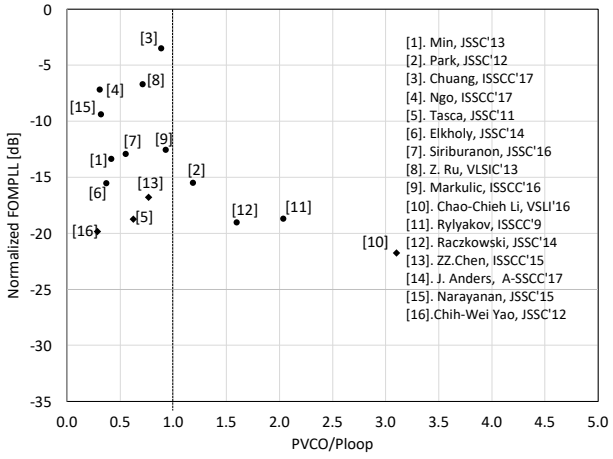


Fig.2. FOM_{PLL} normalized versus VCO and LOOP power distribution

IV. FoM PLL THERMODYNAMIC LIMITS

In the previous section, it was shown that both FOM_{PLL} and FOM_{VCO} are transpositions of (10). Since any PLL is built around a voltage-controlled-oscillator (VCO), it is also useful to see how these two FOMs relate to each other.

By reusing (10), the FOM_{OSC} of the VCO closed into a PLL (FOM_{VCO}) can be expressed as function of the bandwidth of the PLL (f_{BWPLL}) and the jitter accumulated by the VCO outside the bandwidth of the PLL ($\sigma^2{}_{vco}$) which corresponds to an integration time of $1/f_{BW_{PLL}}$.

$$FOM_{VCO} = \frac{\Delta t}{P.\sigma_a^2} = \frac{1}{\sigma^2{}_{vco} \cdot P_{vco} \cdot f_{BWPLL}} \quad (16)$$

where P_{VCO} is the power consumption of the VCO. By combining (16) with (15), FOM_{PLL} can be rearranged as function of FOM_{VCO} as follows

$$FOM_{PLL} = \frac{\sigma^2{}_{vco}}{\sigma_a^2} . \frac{P_{VCO}}{P_{PLL}} . \frac{f_{BWPLL}}{1Hz} . FOM_{VCO} \quad (17)$$

where P_{PLL} is the total power consumption of the PLL. This equation is very intriguing since it allows to identify an upper limit that only depends on the type of the oscillator used and the reference frequency adopted (f_{REF}). In fact, since $\sigma^2{}_{vco}$ cannot exceed σ_a^2, $P_{VCO} < P_{PLL}$, and f_{BWPLL} cannot exceed the reference frequency, the upper limit on the FOM_{PLL} is given by

$$FOM_{PLL,MAX} = FOM_{VCO} . \frac{f_{REF}}{1Hz} \quad (18)$$

The presence of an upper limit that depends on both f_{REF} and FOM_{VCO} suggests that the FOM expressed by Gao in (14) and (15) cannot be used as a metric to compare different PLL architectures since merely starting from a better VCO and a higher reference frequency could lead to a higher FOM_{PLL} even with a less efficient architecture.

The fact that better oscillator and higher f_{REF} help to obtain a better FOM is confirmed by the plot in Fig. 1, where several PLL reported in literature are compared by using (15). As shown in Fig. 1, not only all the design reported in literature are below the upper bound given by (18), but also better FOMs are obtained for higher values of $FOM_{VCO} \cdot f_{REF}$.

V. A FOMs FOR PLL ARCHITECTURES COMPARISON

The analysis proposed in the previous section has shown that the FOM_{PLL} expressed by (15) has some biases when used to compare PLL architectures. By assuming a flat in-band noise profile, Gao at al. demonstrated that to minimize the overall jitter for a given power, the PLL bandwidth must be set to an optimal value ($f_{BWPLL,opt}$) so that jitter, and power consumption of the VCO are half of the total [4]. By using equations (4) and (19) reported in [4], it is also possible to extrapolate $f_{BWPLL,opt}$ for any sub-optimal design to be the following :

$$f_{\mathrm{BWPLL,opt}} = f_{\mathrm{BWPLL}} \sqrt{\left(\frac{P_{vco}}{P_{loop}}\right)} \quad (19)$$

Where P_{loop} is, the power consumed by all the components in PLL loop excluding the power consumed in the VCO. When $\sigma^2{}_{vco}$ and P_{VCO} are both half of the total (17) can be rewritten as

$$FOM_{PLL_{opt}} = \frac{1}{4} . \frac{f_{BWPLL,opt}}{1Hz} . FOM_{VCO} \quad (20)$$

The biasing of the classical FOM_{PLL} from the power distribution between the VCO and the rest of the PLL (P_{loop}) is confirmed by the plot in Fig. 2, where the FOM_{PLL} state of the art have been plotted as function of the ratio between P_{VCO}/P_{loop} (after a normalization by FOM_{VCO} and f_{REF}, to eliminate the biasing produced by the used of different VCO and different reference frequency). As predicted by Gao et al. in [4], the plot confirms that the designs with better FOM are the ones that tend to equalize the two powers.

A. General FOMPLL for architecture comparison

By using the relationship expressed by (19), equation (20) can be rewritten as

TABLE I
PHASE LOCKED LOOP STATE OF THE ART

	[5]	[16]	[13]	[15]	[8]	[14]	[9]	[2]	[3]	[4]
	Fractional-N digital PLL	Fractional-N digital PLL	Fractional-N digital PLL	Fractional-N Subsampling PLL	Integer-N digital PLL LC DCO	Semi-digital Integer-N PLL LC VCO	Fractional-N Subsampling PLL LC VCO	Fractional-N PLL Ring VCO	Integer-N Subsampling PLL Ring	Injection Locked PLL
fref(MHz)	40	52	49	40	55	**123**	40	32	**192**	**150**
Fout(GHz)	4	3.2	3.83	4.42	11.8	0.98	11.72	2.	2.3	0.9
BW PLL(MHz)	0.31	0.95	0.7	4	1	0.5	1.8	2	15	10
Jitter(ps)	0.56	0.23	0.21	0.13	0.21	0.05	0.20	4.07	0.72	0.84
Power PLL(mW)	4.5	17	11.5	6.2	6	131.3	5.6	15.2	4.6	3.8
PN VCO(dBc/Hz)	-121.1	-128.4	-118	-131.8	-123.8	-142	-125.8	-118	-133	-101.6
Delta F(MHz)	3	3	1	10	20.4	1	9.7	10	100	1
Power VCO(mW)	1.73	3.8	5	1.5	2.5	130	2.7	8.25	2.16	0.9
Ploop(mW)	2.77	13.2	6.5	4.7	3.5	1.3	2.9	6.95	2.43	2.9
FOM_{VCO}[1] (dBc/Hz)	181.2	**183.2**	182.7	**183**	175	180.7	**183**	156.4	157	161.1
FOM_{PLL} (dB)	238.5	240.5	242.8	**249.6**	245.8	245.2	**246.6**	216	236.2	235.7
FOM_A (dBJ^{-1})	-28.1	-26	-25.1	**-18.5**	-24.2	-19.9	-19.6	**-17.7**	**-17.3**	-20.3

[1] Power normalized to 1mW (classical FOM VCO used in literature)

$$FOM_{PLL_{opt}} = \frac{1}{4} \cdot \sqrt[2]{\left(\frac{P_{vco}}{P_{loop}}\right)} \cdot \frac{f_{\text{BW PLL}}}{1Hz} \cdot FOM_{VCO} \quad (21)$$

This expression represent maximum FOM_{PLL} (eq. (15)) that a design would reach if the power were equally distributed to minimize the overall jitter. In this way it is possible to compare the different design regarderless of the constraints that lead to an unbalanced power distribution between loop and VCO. However,as shown previously, for a fair comparison among the different PLL architectures, (21) needs to be normalized by FOM_{VCO} and f_{REF}. This yields the following FOM:

$$FOM_A = 10 \log\left(\frac{1}{4} \cdot \sqrt[2]{\left(\frac{P_{vco}}{P_{loop}}\right)} \cdot \frac{f_{\text{BW PLL}}}{f_{ref}}\right) \quad (22)$$

FOM_A (expressed in logarithmic form) can be used to compare architectures independently of the PLL optimization realized by the designer and without being biased by reference frequency and the VCO performance.

The closer FOM_A is to zero, the closer the PLL is to its optimal point. Additionally, this FOM assumes the basic phase noise profile shown in [4] which is only valid for single PLLs and not the cascaded ones.

In table one, some of the most performant PLLs present in literature are reported and compared by using the traditional FOM_{PLL} expressed by (15) and the new FOM_A introduced in this paper. Among all the designs the three best values for each FOM are highlighted.

VI. CONCLUSIONS

The traditional FOM for both oscillators and PLL has been analyzed and derived in a more general form by demonstrating the presence thermodynamic upper bonds. Furthermore, a new FOM has been introduced for the comparison of PLL's architecture, by eliminating the several biases affecting the traditional FOM, such as performance of the VCO, reference frequency and power distribution.

REFERENCES

[1] A. Pathan and A. Liscidini, "Thermal noise limit for time-domain analogue signal processing in CMOS technologies," in Electronics Letters, vol. 52, no. 18, pp. 1567-1569, 9 2 2016.

[2] Enz, C., and Vittoz, E.: 'CMOS low-power analog circuit design'. Proc. of IEEE Int. Symp. on Circuits and Systems (ISCAS), Ch. 1.2, Tutorials, Atlanta, May 1996, pp. 79–133

[3] B. Murmann, "The Race for the Extra Decibel: A Brief Review of Current ADC Performance Trajectories," in IEEE Solid-State Circuits Magazine, vol. 7, no. 3, pp. 58-66, Summer 2015.

[4] X. Gao, E. A. M. Klumperink, P. F. J. Geraedts and B. Nauta, "Jitter Analysis and a Benchmarking Figure-of-Merit for Phase-Locked Loops," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 2, pp. 117-121, Feb. 2009.

[5] D. B. Leeson, "A simple model of feedback oscillator noises spectrum," Proc. IEEE, vol. 54, pp. 329–330, Feb. 1966.Razavi book

[6] A. A. Abidi, "Phase Noise and Jitter in CMOS Ring Oscillators," in *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1803-1816, Aug. 2006.

[7] M. Garampazzi, S. Dal Toso, A. Liscidini, D. Manstretta, P. Mendez, L. Romanò, and R. Castello, "An intuitive analysis of phase noise fundamental limits suitable for benchmarking LC oscillators," IEEE J. SolidState Circuits, vol. 49, no. 3, pp. 635–645, Mar. 2014.