A Noval Area Efficient Low Voltage & Low Power Voltage Controlled Oscillator Using Hybrid CMOS Technology.

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***Abstract*— This paper shows low power dissipation, a hybrid CMOS VCO (Voltage-Controlled Oscillator) with a linear response over a wide power range. CMOS NAND three-transistor gates were used to design CMOS voltage-controlled oscillators. CMOS VCOs have been suggested for three, five, and seven stages in the conception of ring-based CMOS VCO circuit, and new delay cell with three CMOS NAND transistor gates. With supply voltage 0.7V. The output frequency was regulated. CMOS VCO frequency, power dissipation, and hybrid CMOS (VCO) voltage-controlled oscillator (VCO) are investigated in three-, five, and seven stages. A hybrid CMOS-VCO device combination is used to hybrid ion the VIC response without the need for a resistor or wide device. Compared with CMOS pure circuit with 0.7V tuning and control voltage, the circuit shows excellent linearity.**

***Keywords*— *Voltage Controlled Oscillator, CMOS, Operating Frequency, Power consumption, Cadence*.**

I. INTRODUCTION

Building blocks used by electronic circuits with combined and analog signals, including Analog to Digital Converters (ADCs), Phase-Locked Loops (PLLs), and several others, VCO is an analog, mixed-signal electronic circuit building block commonly used [1],[2]. Mainly topologies like VCOs and LC tank oscillators are part of VOC designs. In PLL applications, VCOs have a comparatively wider tuning range; smaller silicone regions in contrast with LC oscillators, and are ideally suited to silicone integration [3]. In comparison with the VCO spring oscillator, the designs of the LC tank oscillating with PLL are however better noise phase efficiency [5] [4]. The current CSVCO (current starved voltage controlled oscillator) is a topology used oscillator-based VCO topology, Comprising several stages VCO like a starved current oscillator and inverter stages controlled by voltage [6]. Schmitt triggers with hysteresis and a single inverter, consisting of a single VCO step, resulting in fewer circuit transistors, in comparison to CSVCO. We propose a hybrid voltage regulated oscillator of Schmitt's CMOS and CNFET-Ansatz in this paper. In comparison to pure CMOS circuits, the proposed hybrid circuit is designed for improved linearity and reduced dissipation of power. In the HSPICE environment, simulations of the proposed VCO are carried out. CNFETs function as an outstanding active transistor interface channel because of very high electron mobility, successful transport of carriers, also enhanced gate electrostatic carbon nanotubes [7][8]. CNFETs were not only thoroughly examined on basic integrated circuits, such as logic portals and ring oscillators, in the sense of different analog and RF (radio frequency) circuits. Recently the CNFETs have shown that highly linear RF circuits and application candidates are promising. Researchers in [9] demonstrate that the linearity of CNFETs is comparable to typical MOSFETs. Various researchers faced the hybrid development, using conventional MOSFETs and modern nanoelectronic systems, of electronic circuits. Hybrid 3D CMOS-CNFET inverters integration is suggested in [10] study. In the application for the co-integration of NMOS and PCNFET cascade amplifier RF, researchers from Stanford University reported [11]. A hybrid CMOS-CNFET chemical sensing application is specified in [12]. In CMOS transistors to be replaced for power, gating is suggested CNFETs [14]. The new monolithic 3D integration of computer elements, memory, RF, and analog building block will enable nanoelectronic systems to become more future-proof. Such 3D integrated systems have been shown in [15] as hybrid cointegration of CNFET logic building blocks and traditional CMOS silicon blocks, in which researchers have answered vertically stacking integrated circuit layers.

II. CIRCUIT DESCRIPTION

Return to the first stage entry last stage ring-based oscillator design output. Figure 1 shows a single-stage N-delay inverter VCO block diagram. In the event of an oscillation, an alteration of the phase of 2β and voltage increase of the unit must be accomplished. Return to the first stage entry last stage ring-based oscillator design output. Figure 1 shows a single-stage N-delay inverter VCO block diagram. In the event of an oscillation, an alteration of the phase of 2β and voltage increase of the unit must be accomplished. Any late cell in which N is the total number of delay phases should be specified for a phase shift of Ţ / N. The dc reversion of the inverter delay cell provides the remainder of the λ phase shift. The odd number of delay phases is critical for dc inversion in single-end oscillator design. fo = 1/2Ntd is VCO oscillation frequency, N is total no. of delay steps & td is a delay for every stage. Various kinds of delay cells, single-ended delays, & Dual-delay paths, including multi-feedback loops, have been reported in transducer design literature. Delay cell strategies have been used, coupling cells, such as inverter stages, latches, etc. Delay phases are basic building blocks for every VCO model also their improved nature affects the total performance of the VCO model. This paper proposes a new delay cell, which takes into account the significance of energy consumption and the frequency range.

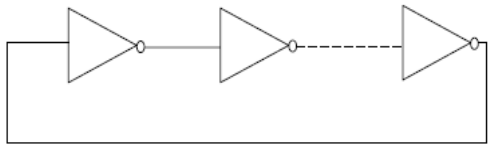

Fig.1: Block diagram of N-delay Inverter Single-ended VCO.

The VCO o/p frequency of the ring is based on the time every delayed cell inverter provides. The NAND-based delay cells use three transistor gates in the proposed designs. The three-transistor NAND gates shown in Figure 2 were operated by an inverter.

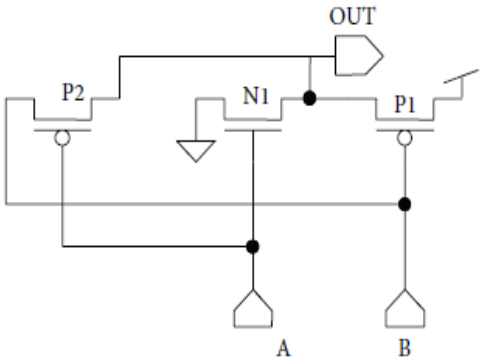

Fig.2: 3-Transistor CMOS NAND gate.

III. Proposed CMOS VCO Circuits and Hybrid CMOS VCO

The circuits were equipped with a 0.7V supply voltage of 90 nm CMOS technology. The delay cells have removed the direct path between Vdd and field, thus increasing leak power and providing energy-efficient designs. Two PMOS transistors and one NMOS are made of NAND delay stages. Logic 1 (i.e. 1.0V) from two NAND gate input terminals is connected with one, and the signal of feedback is extended to other terminals. This circuit acts as an inverter without a direct path between Vdd and soil saving energy. The length of the gates of all three transistors is 0.9 µm. Transistor NMOS (N1) Diameter (Wn) is 1.20 µm. Transistor width (Wp) of P1, P2 is 1.20 µm. Differences in supply voltage (Vdd) from stages of NAND delays have controlled output frequency. CMOS VCOs were designed and simulated for three, five, and seven levels; VCOs were also designed with a similar concept for seven stages. The proposed NAND gate has 3 transistors, making the design more efficient with 4-transistors & less crowded than usual NOR or NAND gates. The proposed design of the NAND gate depends upon transistor logic that decreases the internal capacity and is appropriate for circuit power output. The design of the NAND gate eliminates direct connection to Vdd and only one NMOS transistor is linked to the field, which makes the design more effective than conventional gate design.

The proposed circuit is studied for frequency, dissipation of electricity produced in sense of variations of parameters such as control voltage (CV), VCOs of Ring Oscillator comprise n phases, each contributing to general nonlinearity of VCO. Compared with pure CMOS circuits, the hybrid circuit has a stronger linear response. Due to the use of high Vth devices in reducing power dissipation, the nonlinear response in pure CMOS is NAND-dependent delays have been planned and simulated in three stages, five-stage with NAND-based delays, seven-stage with NAND-based delay, and Hybrid CMOS VCOs.

IV. Simulation Work

A. Three-Stage with NAND based Delay

Two PMOS semiconductors and one NMOS are semiconductors of the NAND postpone stage. One is related to logic 1 (such that, 1.0V) from two NAND gate input terminals, on other terminals, a feedback signal is applied. This circuit acts as an inverter between Vdd and soil that saves energy without immediate means. The NAND gate proposed has three transistors, making its architecture more efficient and less cramped than conventional 4-transistor NAND or NOR gates. The 3-stage schematic of CMOS VCO appears in Fig.3 and the output waveform in Fig.4 is shown.

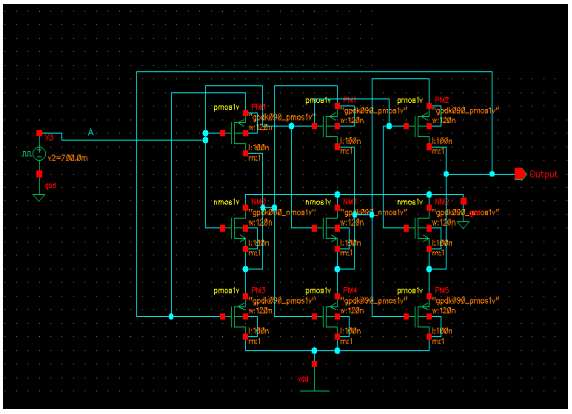

Fig.3. Schematic of 3-stage CMOS VCO

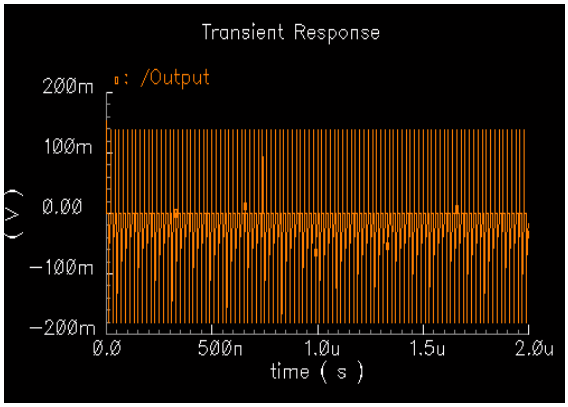

Fig.4. the output waveform of 3-stage CMOS VCO

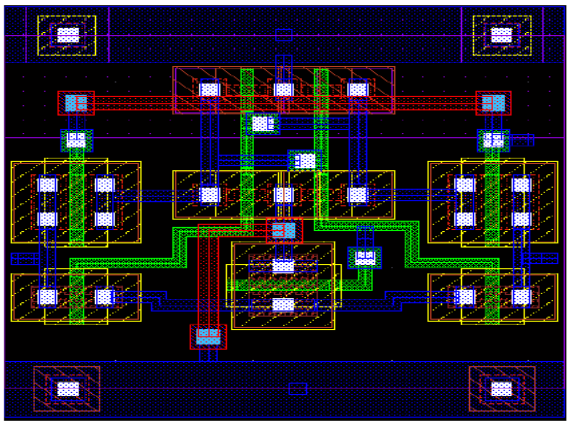

Fig.5. The layout of 3-stage CMOS VCO

B. Five-Stage with NAND based Delay

Two PMOS transistors are NAND phase delay transistors and one NMOS transistor. One is connected to logic 1 (such that, 1.0V) from two NAND gate input terminals, and the next terminal is added to the critical signal. This circuit acts as an inverter between Vdd, ground sparing force without an immediate way. Fig. 6 shows a 5-stage plan of CMOS VCO, Fig.7 demonstrates the o/p waveform.

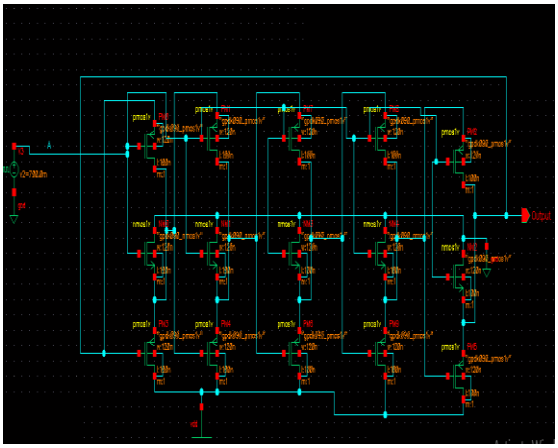

Fig.6. Schematic of 5-stage CMOS VCO

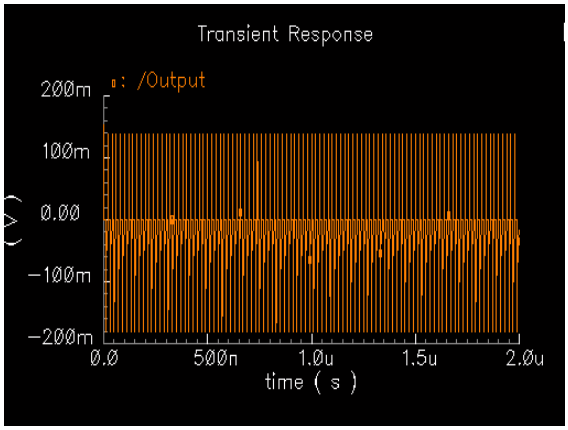

Fig.7. the output waveform of 5-stage CMOS VCO

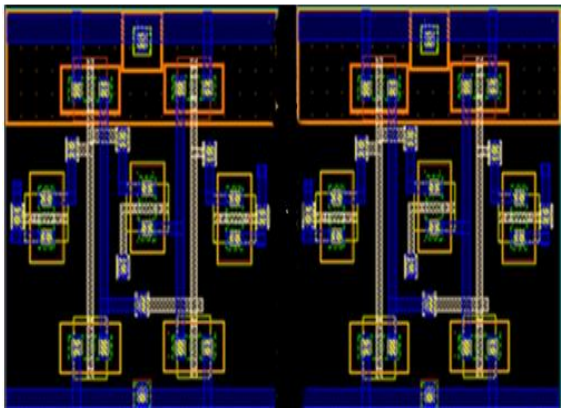

Fig.8. The layout of 5-stage CMOS VCO

C. Seven-Stage with NAND based Delay

Two PMOS transistors and one NMOS are composed of NAND delay points. One is connected by two NAND gate input terminals to logic 1 (i.e. 1.0V), The control framework is used for other terminals. This circuit operates without a direct path between Vdd and ground-saving power as an inverter. Fig.9 displays the CMOS VCO schematic and the output wave shape is shown in Fig.10.

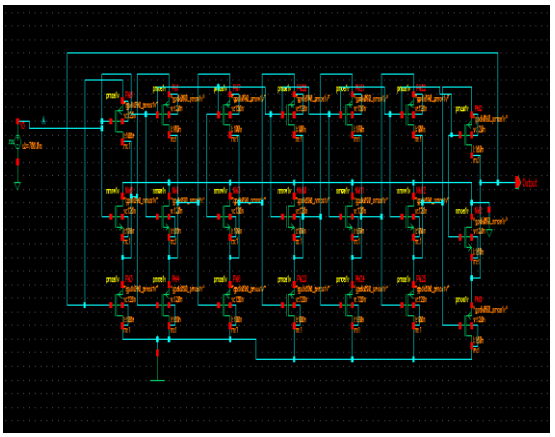

Fig.9. Schematic of 7-stage CMOS VCO

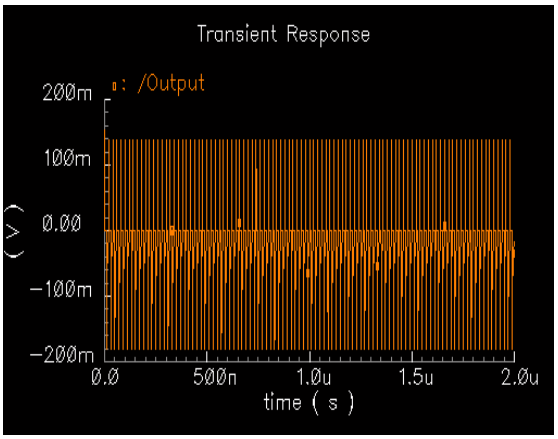

Fig.10. the output waveform of 7-stage CMOS VCO

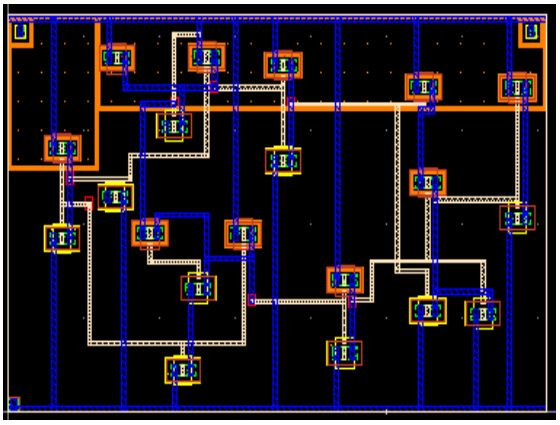

Fig.11. The layout of 7-stage CMOS VCO

D. Hybrid CMOS Voltage Controlled Oscillator (HCVCO)

Following parameter variations, such as control voltage (CV), for induced frequency & power dissipation, the circuit is investigated. VCOs of ring oscillators consist of an n-number of the stage, with total nonlinearity of VCO at each stage. The topology given in Figure 12 can be used to resolve this problem by using one single current stage of starvation followed by hysteresis trigger Schmitt. An RC oscillator is one of the applications of a Schmitt trigger. Similarly, Schmitt can form a voltage-controlled oscillator along with current sources. For the construction of the Schmitt trigger, the proposed design utilizes Hybrid CMOS. HCVCO also

reflects current sources in MOSFETs PM0 and NM6. PM2 and NM0 are transistors. The inverter is made with normal MOSFETs. The hybrid implementation of MOSFETs is W/L=1.2. One of VCO's most important criteria for PLL applications is broad & linear tuning range. In contrast to pure CMOS, better linear response from the hybrid circuit. In a pure CMOS circuit, a non-linear response is because high Vth devices used to cut power dissipation output of Hybrid CMOS VCO waveforms are shown in Figure 13.

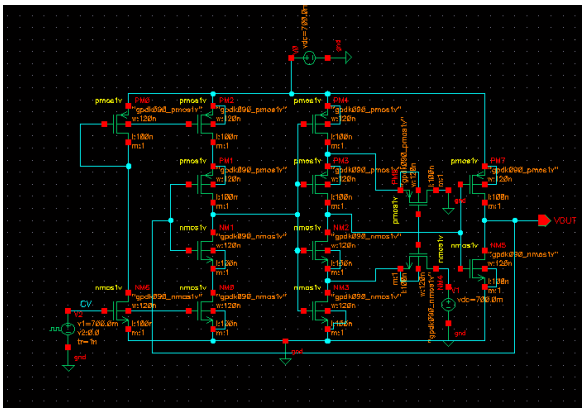

Fig.12. Schematic of Hybrid CMOS Voltage controlled oscillator (HCVCO)

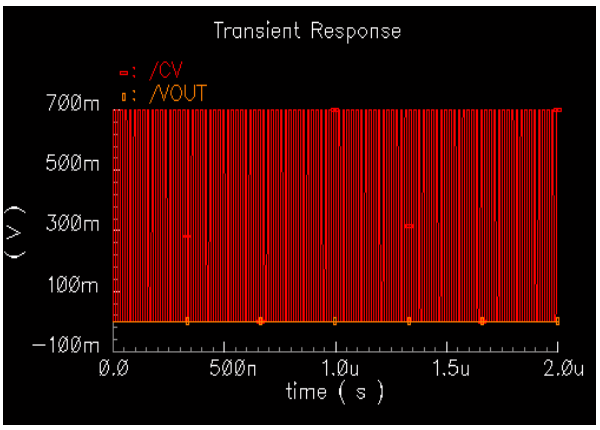

Fig.13. The output waveform of HCVCO (Hybrid CMOS Voltage Controlled Oscillator)

V. Result and Discussion

For all the designs the simulation and synthesis are done. CADENCE tool with nominal supply voltage Vdd=0.7 V is a 90 nm technology for the evaluation of the performance of existing adder designs as well as of the proposed 3-stage, 5-stage, 7-stage CMOS VCO and Hybrid CMOS VCO designs. Delay cells have eliminated the gate leakage, as the only mechanism dominant at room temperature 27 ° C Direct path between the Vdd and ground, All parameters such as leakage power and frequency are tabled, so power leakage is decreased & designs are efficient.

TABLE I. Comparison of CMOS VCO and HCVCO Performances

Performance Parameter	**Proposed 3-stage CMOS VCO**	**Proposed 5-stage CMOS VCO**	**Proposed 7-stage CMOS VCO**	**Proposed Hybrid CMOS VCO**
Technology Used	90nm	90nm	90nm	90nm
Supply Voltage	0.7V	0.7V	0.7V	0.7
Power consumption	12.32µW	21.43µW	32.68µW	11.09 µW
Operating Frequency	4.9GHz	3.6GHz	2.7GHz	4.8GHz
Transistor used	9	15	21	14

VI. Conclusion

CMOS ring CMOS VCO designs with three-transistor NAND gates were improved in recorded work. CMOS VCOs with 3, 5, and 7 stages with reduced power consumption have been published. The frequency, power dissipation, and comparison with hybrid CMOS voltage-controlled oscillators (VCOs) were investigated at three-stage, five-stage, and seven stages CMOS VCOs. A hybrid CMOS-VCO device combination is used to linearize the VCO response, without requiring a resistor or wide device. In comparison to the pure CMOS circuit, the circuit shows excellent linearity through a 0.7V tuning and control voltage. With supply voltage 0.7V, the output frequency is controlled. As one of the most important requirements, Wide and linear tuning range of VCO for PLL applications. In contrast to pure CMOS, the hybrid circuit provides better linear response and less area. Our strategy shows substantial power savings with a large tuning range, in comparison to the previously reported design.

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