Closed Loop Control with SVPWM and Performance Evaluation of Reduced Part Count Multiverter Inverter Interfacing Three Phase Grid Connected PV System

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CLOSED LOOP CONTROL WITH SVPWM AND PERFORMANCE EVALUATION OF REDUCED PART COUNT MULTILEVEL INVERTER INTERFACING THREE PHASE GRID CONNECTED PV SYSTEM

N.RAMESH(Assistant Professor), CH.TEJASWINI, A.RATNAKAR, G.HANISH

Abstract :In the power sector, multilevel inverters(MLIs) have drawn tremendous attention. Use of multilevel inverters have been growing extensively to improve the power quality and efficiency of the photovoltaic (PV) system, For an MLI interfacing PV system, the size, cost and voltage stress are the key constraints of the MLI that need to be minimized. This project presents a novel reduced part count MLI interfacing single-stage grid-tied PV system along with a closed-loop control strategy. The proposed MLI consists of n repeating units and a level boosting circuit (LBC) that helps in generating 4n + 7 voltage levels instead of 2n + 3 levels. Three different algorithms are proposed for a proper selection of dc-link voltages to enhance the levels further. A comparative analysis is carried out to confirm the superiority of the developed MLI. The workability of the proposed MLI is investigated with a 1.3 kW PV system. The closed-loop control strategy ensures the maximum power tracking, dc-link voltage balancing, satisfactory operation of the MLI and injection of clean sinusoidal grid current under any dynamic changes. Comprehensive simulation analysis is carried out considering a 15-level MLI structure. Experimental tests further confirm the practicality of the topological advancement for a PV system under different dynamic conditions.

Keywords : Multilevel inverter,distributed maximum power point tracking,assymetrical repeating unit, photovoltaic(PV) system

I. INTRODUCTION

Research attempts for the development of renewable energy-based power generation systems integrated with multilevel inverter (MLI) are burgeoning. These systems developed for both the standalone and grid-tied applications. The primary goal of such systems is to attain full power with reduced harmonic distortion, low power loss, and low volt- age stress, unlike the commonly used three-level inverter. In retrospect, the cascaded H-bridge (CHB) MLI structures employed extensively interfacing with photovoltaic (PV) systems for higher reliability and easy modularity. Consequently, higher power rating and higher voltage lev- els achieved as per the requirement. CHB MLI requires multiple isolated dc sources in each H-bridge, thus mak- ing it highly suitable for PV application as individual PV panel used in each H-bridge along with distributed maximum power point tracking (DMPPT) control. It can help in har- vesting maximum energy from the PV sources. On the contrary, single dc source-based MLIs such as diode-clamped and capacitor-clamped MLI demands several components and complex control circuitry to synthesize mul- tilevel output [9], [10]. The shortcoming of conventional MLIs is the involvement of a higher number of power devices.

2. PROPOSED SYSTEM CONFIGURATION

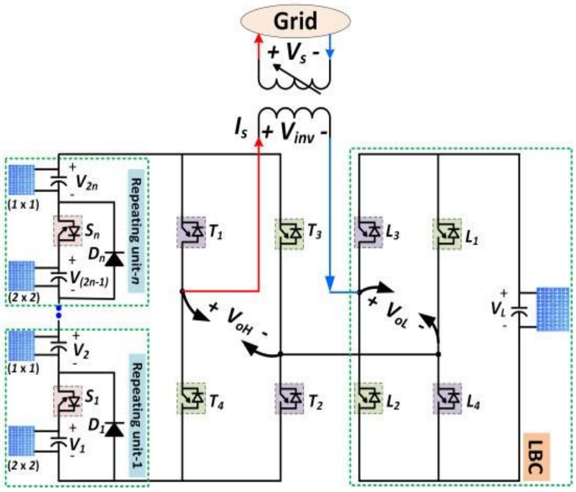
The generalized structure of the proposed voltage level boost (VLB) MLI for the single-stage grid-connected PV system shown in Fig. 1. As indicated, VLB MLI is the combination of three modules such as; repeating unit (RU), H-bridge, and LBC. RU consists of two PV strings as input sources which can be repeated in a series manner to achieve higher voltage levels. Moreover, the inclusion of LBC in the VLB MLI exactly doubles the number of levels with the addition of four extra switches. Numbers of switches (N_{sw}), the number of sources (N_{dc}) and the number of diodes (N_{dd}) involved in the VLB MLI in terms of RU (n) are expressed in (1-3). In this work, the VLB MLI is integrated with the grid through a small size low pass filter (inductor) to reduce further the current harmonics caused by switching action.Three different algorithms to select input source.

.Proposed MLI interfacing grid-tied PV system.

Number of switches (N_{sw}) $= n + 8$

Number of input sources (N_{dc}) $= 2n + 1$

Number of diodes (N_d)



A. PROPOSED ALGORITHMS (PA)

Magnitudes of the dc-links for RUs are selected as perthe algorithms presented in Table 1.Magnitudes can be selected as asymmetrical, arithmetic and binary ratio accord-ing to PA1, PA2 and PA3, respectively. The generalized expressions for the output voltage levels ,TBV,and switching loss in terms of Rus also included.This work analyzes the performance of the VLB MLI considering PA1.The VLB MLI produces a 15-level output with PA1 when two Rus are taken into consideration.The source used in the LBC is responsoible for the generation of the first step while the second step is produced by turning off the switches in the RU along with deactivating the LBC.The third step can be obtained by activating the LBC soure.Afterwards, Rus are switched to generate the fourth step and the further.For the 15-level case, blocking voltages across each switch is illustrated in the below figure.Performance of VLB MLI with the three proposed algorithms is illustrated.

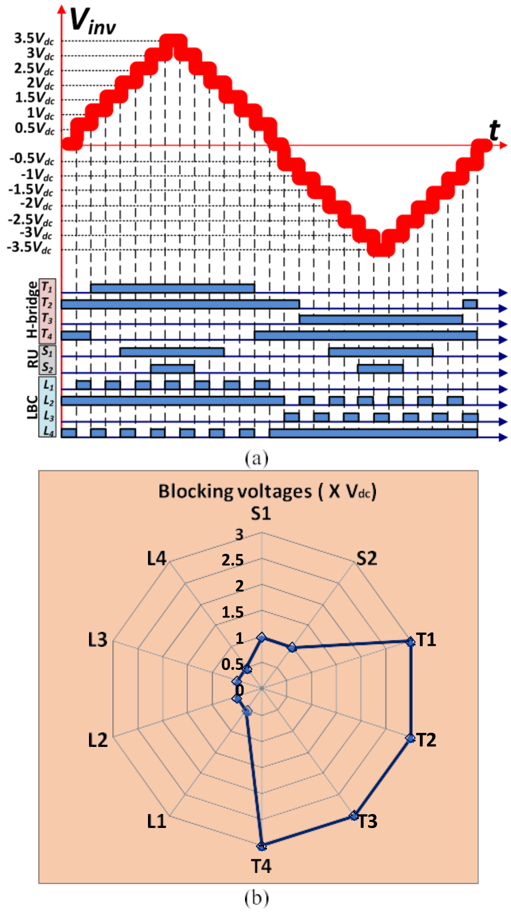


FIGURE.1 (a) Switching states for producing 15-level output.FIGURE (b) Blocking voltages of the individual switch for the 15-level MLI.

COMPARATIVE ANALYSIS

The prime purpose of the current work is to devise a novel MLI structure having lesser switch count and TBV. To val- idate the competence, the proposed VLB MLI is compared with different MLI topologies developed recently. Hereafterthe MLI topologies in [18], [28], [38], [23], [36], [29], [37], [26] are termed as T1, T2, . . . , T8. The MLI presentedin [26] utilizes a higher number of switches but reduces the source count. The MLIs presented in [29], [36], [37] employs lesser switch count than a conventional CHB the proposed VLB MLI .

Addition of more number of dc sources will result in more number of voltage levels, but at the same time, TBV will increase. The MLI topologies developed in [26], [28], [29], [38] involves a single dc source and additional capac- itors for generating multiple voltage levels. All these MLI topologies are corroborated for lower-level applications. Although TBV becomes less for these MLIs, but voltage bal- ancing issue and control complexity may arise in higher-level applications. It is clear from Fig. 4(c) that, the proposed VLB MLI requires a lesser number of dc sources to synthesize the same level output. Fig. 4(d) shows there is no need for additional capacitors in the proposed MLI. Further, CLRis calculated for all the MLI topologies for evaluating a generic cost comparison. CLR is the ratio of sum of the cost deciding parameters (N_{sw}, N_d , N_c, N_{dc}, and the number of driver circuits) with N_l. In this perspective, the VLB MLI exhibits a lower value of CLR among all the considered MLIs, as shown in Fig. 4(e) which indicates the cost-effectiveness of the proposed structure.TBV is an important parameter which decides the applica- bility of an MLI in high voltage. In order to compute the TBV, the blocking voltages of all the individual switches are addedtogether.

4. CONTROL STRATEGY

The 15-level VLB MLI utilizes two varieties of dc-link voltages ($0.5V_{dc}$ & V_{dc}). Thus it is most important to con- trol the dc-link voltage so that they can be maintained at desired values. In this aspect, a suitable close loop con- trol strategy has been employed for the grid-tied PV fed VLB MLI system with critical objectives such as maxi- mum power extraction from the PV-array, dc-link voltage balancing under dynamic change in insolation, injection of clean sinusoidal grid current at unity power factor, control of overall system under phase change and grid side per- turbations. The comprehensive control system is shown in Fig. 5.

A. *MPPT CONTROL*

The performance of the PV systems is highly dependent on the temperature and insolation level, which are not uniform throughout the day. For harvest maximum power, MPPT control technique is adopted, which will make the sure operation of PV at MPP. Although various MPP tracking techniques have been investigated in literature [39], [40], incremental conductance MPPT [13], [40] is implemented due to its full viability and simplicity. The MPPT control then produces the reference voltage signal for the voltage control loop. For efficiently extract maximum PV power under insolation mismatch conditions, DMPPT control is performed, i.e., MPP tracking is carried out in each RUs. The required reference current is further generated by com- paring the actual individual PV voltages with the total PV voltage.

B.TOTAL VOLTAGE CONTROL LOOP

Closed-loop voltage control is employed to maintain the total dc-link voltage corresponding to the reference set voltage considering any change in PV characteristics. The control loop calculates error taking the sum of theactual/measured dc-link voltages (V_{total}) and the sum of individual reference dc-link voltages ($V_{total}*$) that are gen- erated from the MPPT control algorithm. The obtained voltage error is minimized by processing it through a proportional-integral (PI) controller. The parameters (K_{p1}, K_{i2n}) of this PI-controller are tuned so that the peak value of the injected grid current becomes maximum. Further, a phase-locked loop (PLL) is used to synchronize with the gridfrequency.

C.INDIVIDUAL VOLTAGE CONTROL

Although the total voltage controller module maintains the total dc-link voltage at the desired value, but individual dc-link balancing is not guaranteed. Therefore, an individual control loop is also used for balancing each dc-links. The output of each individual voltage control modules is used togenerate the reference signal for PD-PWM controller of VLB MLI.

D.CURRENT CONTROL LOOP

For obtain the desired power balancing in addition to the voltage control, a current controller is used to maximize the PV output. This current control loop generates the cur- rent error by comparing the reference grid current (I_S*) and the actual/measured grid current (I_s) which is then processed through a PI-controller.

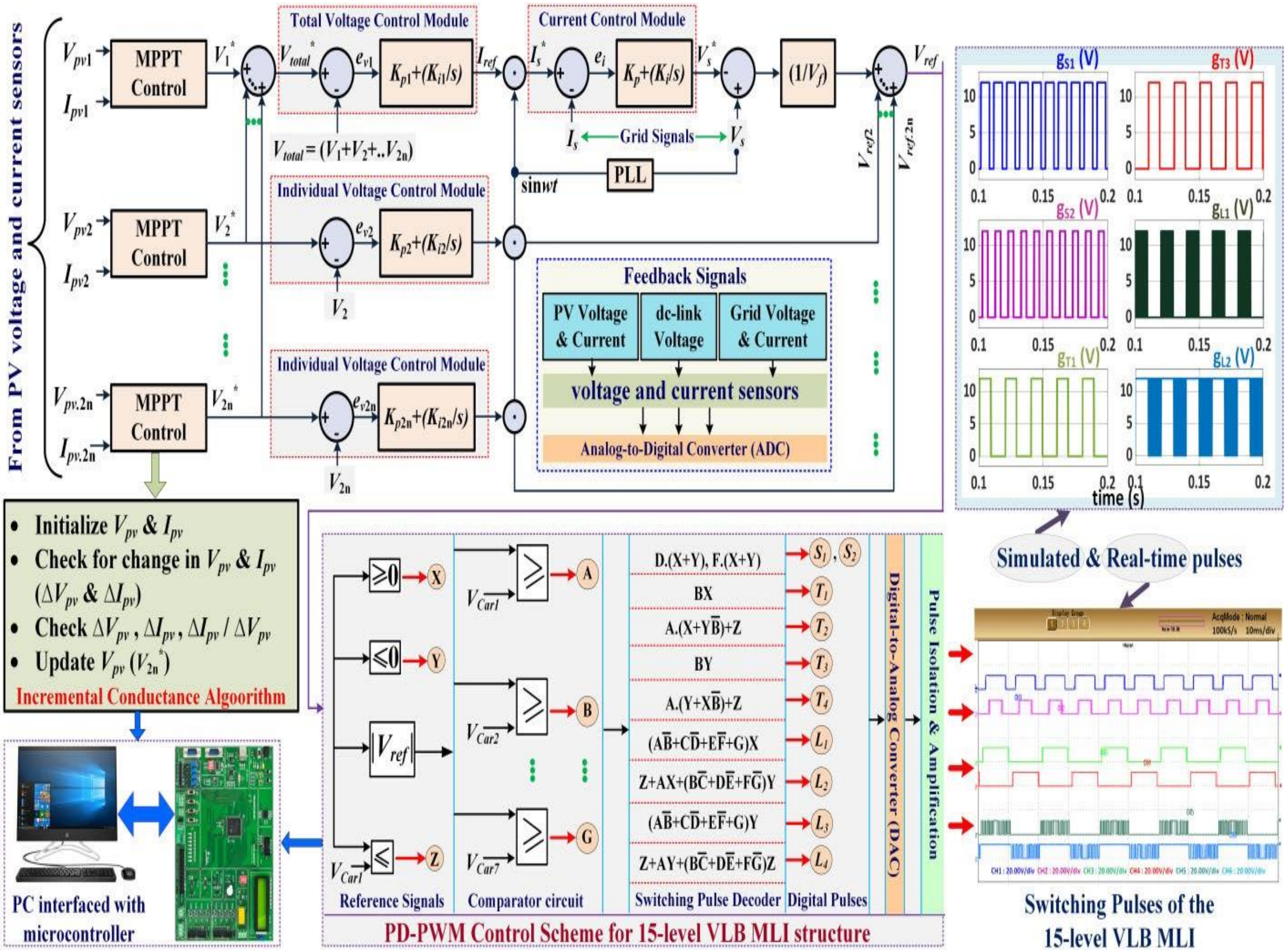


figure 2.Closed loop control scheme for the proposed grid-tied PV system

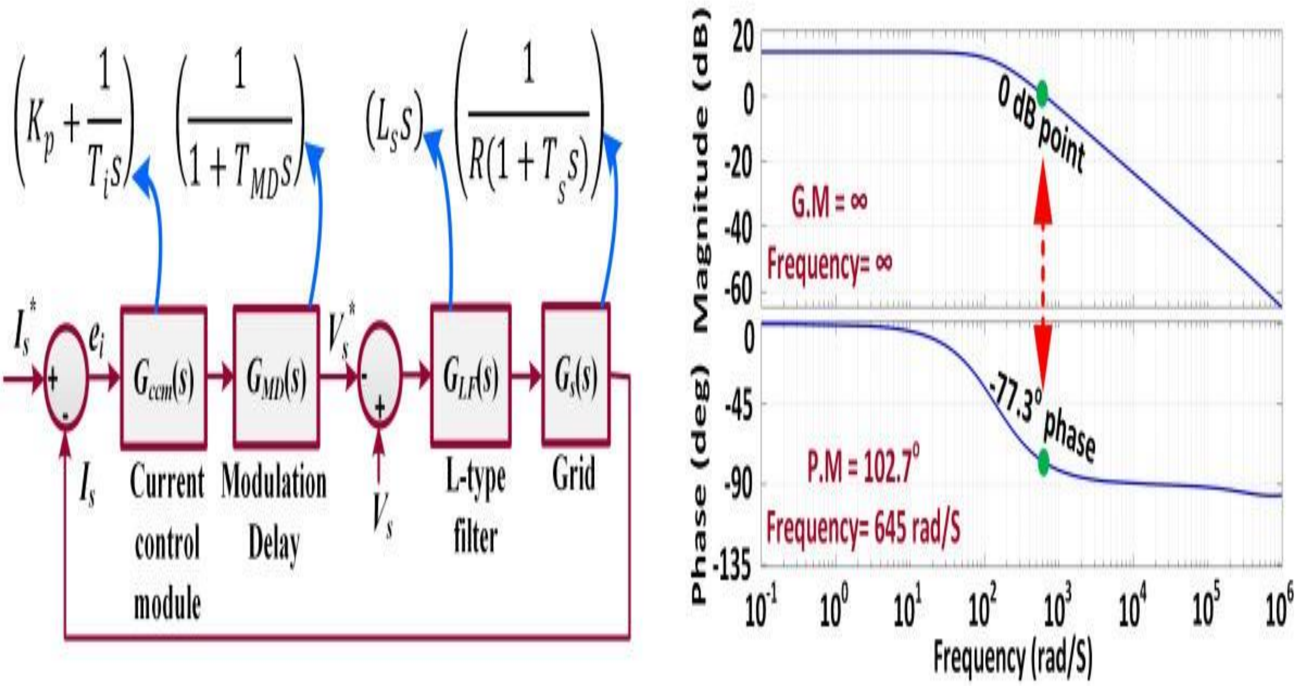


figure 3..Equivalent block diagram of the closed loop current controller & stability performance

The parameters of the PI-controller (K_p, K_i) are tuned for optimizing the error.The output of this controller is compared with the gridvoltage (V_s) for generating the reference voltage of the inverter for any change in V_s. Accordingly, the invertervoltage follows the grid voltage under every unwanted circumstance.

E.PHASE-DEPOSITION PWM CONTROL OF VLB MLI

The phase-disposition PWM (PD-PWM) control scheme canbe implemented in three stages such as; reference signal generator, a comparator circuit, and switching pulse decoder.For an MLI to produce N_l level output, (N_l 1)/2 number of triangular carriers are required for the aforesaid control mech- anism [10]. Thus, seven carriers are disposed of in-phase witha precise offset level for the 15-level VLB MLI. Thereby, the carriers are compared with the reference sinusoidal sig- nal in the comparator circuit for producing seven switch-ing states. The switching pulse decoder circuit comprises ofseveral digital logic gates then generate pulses considering switching logic.

F.STABILITY ANALYSIS

The stable functionality of the adopted closed-loop con-troller for the proposed grid-tied system [11] is examined in this section. The overall equivalent block diagram shown in Fig. 6 is considered for stability analysis. The overall transfer function (TF) of the proposed system in Laplace domain ($G(s)$) is computed taking the product of TF of cur- rent control module ($G_{ccm}(s)$), modulation delay ($G_{MD}(s)$), grid ($G_s(s)$), and L-type filter (G_{LF} (s)). The value of the pro-portional gain (K_p) & integral gain (K_i) of the current control module is taken as 0.7 & 10, respectively. The integral time constant (T_i) is the reciprocal of K_i. The time of modulation delay (T_{MD}) is considered as 1.5 times of sampling time (T_s). Fig. 6 also depicts the bode plot stability analysis of the considered system. The phase margin (PM) is computed to be 102.7° and the phase plot stabilizes much ahead of 180°. Therefore, the gain margin (GM) of the proposed system is infinite. It may be concluded from the figure that both GM & PM values are more significant than zero, which verifies a stable control strategy.

Standard insolation & temperature	1 kW/m^2, 25° C
Total PV array power (P_{pv})	1.375 kW
Maximum power of PV panel (P_{mp})	125 W
Open circuit voltage of PV (V_{oc})	21.4 V
Short-circuit current of PV (I_{sc})	7.6 A
Voltage & current at P_{mp} (V_{mp}, I_{mp})	17.7 V, 7.1 A
Panel efficiency	16.3 %
No. of series, parallel modules (N_{s1}xN_{p1}), (N_{s2}xN_{p2})	(2x2), (1x1)
Grid voltage (V_s)	90 V (peak)
Grid impedance	0.7 Ω-5 mH
dc-link capacitors	1500 μF, 2200 μF
Filter inductance (L_s)	4.7 mH
Inverter output & switching frequency (f_o, f_{sw})	50 Hz, 5 kHz

TABLE : SIMULATION &EXPERIMENTAL DESIGN PARAMETERS.

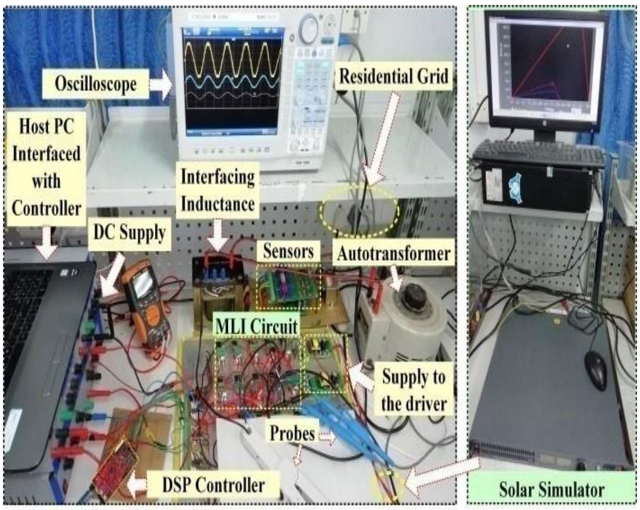
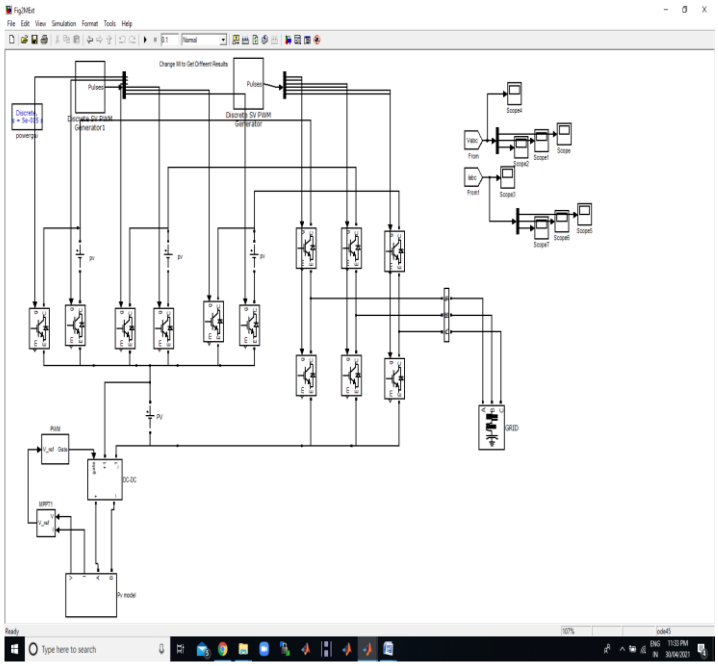


FIGURE 4.Experimental test setup of the proposed system.

5.SIMULATION ANALYSIS

In this section, the operation of 15-level VLB MLI in single-stage grid-tied PV system under MATLAB/Simulink environment is investigated. The adopted closed-loop control strategy as outlined earlier makes sure maximum PV power extraction and the dc-links are maintained at desired voltage levels ($0.5V_{dc}$ & V_{dc}). PV panels are connected to the VLB MLI through the 1500 μF & 2200 μF dc-link capacitors. The values are chosen, considering 2-3 % voltage ripple and nominal output frequency. The carrier frequency and reference sinusoidal frequency are chosen as 5 kHz & 50 Hz. Several 125 W PV panels arranged in (2 $\times$ 2) and (1 $\times$ 1) are considered as an input source for the VLB MLI to obtain the desired dc-link voltage V_{dc} & $0.5V_{dc}$, respectively. The parameters considered in the simulation are given in Table 3. Fig. 8(a) shows the output voltage of the proposed VLB MLI (V_{inv}) and injected grid current (I_s) at different MI values ($MI = 0.5$, $MI \approx 1$, $MI > 1$). With the decrease in MI value, the MLI is able to operate at a reduced voltage level. On the other hand, overmodulation ($MI > 1$) causes distortion in voltage waveform. Hence, it is always desirable to operate near unity MI value. Fig. 8(b) depicts the harmonic spectra of the output voltage of the MLI and grid current. The % THD values of both output voltage and current waveform are below 5% obeying the IEEE-519 standard. Tests are further conducted under different dynamic con- ditions. Fig. 8(c) shows the results with varying insolation at 0.12 s to 300 W/m^2 from 750 W/m^2. During this, the grid.Tests are fvoltage (V_s) remains unaffected; however, grid current mag- nitude changes accordingly with insolation change. MPP tracking performance is also delineated in Fig. 8(d). The dc-link voltage is automatically tracked to the reference value and maintained at the desired level even under a change in insolation level. Voltage sag is a common incident in the power system network which is generally caused by faults inthe transmission line, sudden load change or excessive load demand. Under voltage sag initiated at 0.4 s, Fig. 8(e) also shows the grid current increases to an extent which ensures the power balance, *i.e.*, the injected power to the grid is main- tained Moreover; the PV fed VLB MLI continuously injects a clean sinusoidal current to the grid even under 0.94 lagging power factor (PF) condition as shown in Fig. 8(f). However, the proposed converter can result in unsatisfactory perfor- mance under very low PF due to the presence of discrete diodes in the conducting path.

SIMULATION CIRCUIT:



EXPERIMENTAL VERIFICATION:

The real-time operation of the proposed VLB MLI in grid-connected mode is verified on a prototype developed inthe laboratory, as shown in Fig. 7. The 12N60A4D insulatedgate bipolar transistors (IGBTs) and RGP30D discrete diodes are used to build the power circuit. According to the current laboratory availability, one SAS 120/10 solar simulator and four variable dc sources are used as input sources to mimic the PV panel characteristics. Solar simulator and dc sources voltage magnitudes are so adjusted according to Table 3. The output of the VLB MLI is connected to the residential grid through an auto-transformer which steps down the grid voltage to match with the inverter output such that the currentfrom the PV fed MLI can be continuously injected to the grid. LA-55p and LV-25 hall-effect sensors are used to sense the current and voltage, respectively. A DSP controller is used to implement the control technique. Generated pulses are further amplified using TLP250 drivers.

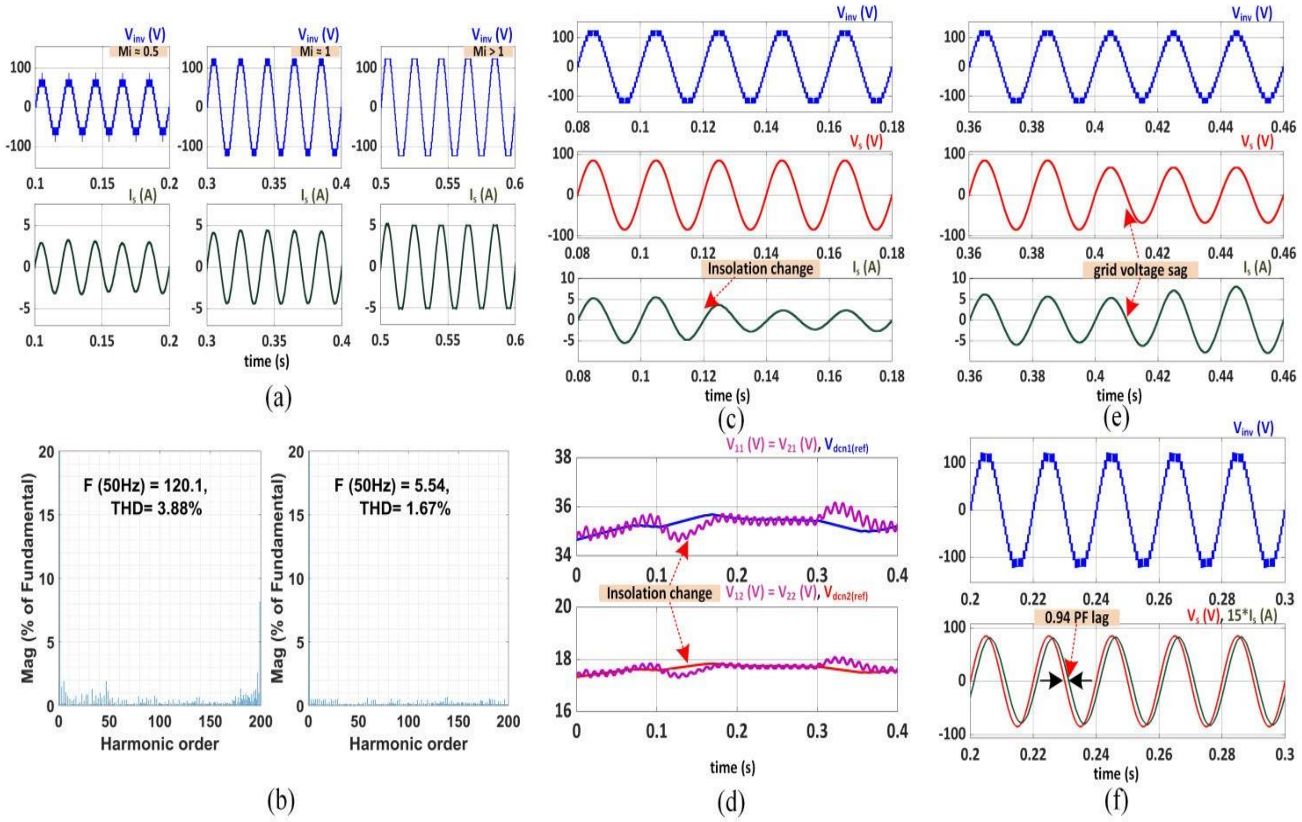


FIGURE 5. Simulation results of the PV fed VLB MLI: (a) V_{inv} & Is under different MI values, (b) Harmonic spectra of V_{inv} & Is, (c)V_{inv} , Vs, Is under varying insolation, (d) dc-link voltages, (e) V_{inv} , Vs, Is under grid voltage sag condition, (f)V_{inv} , Vs, Is under lagging PF.

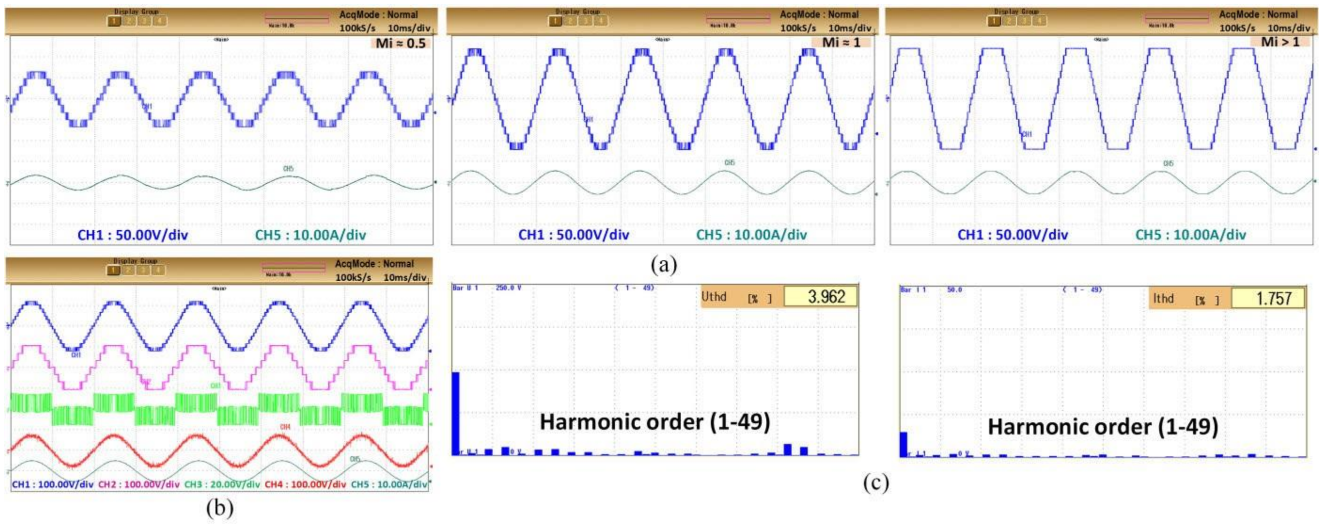
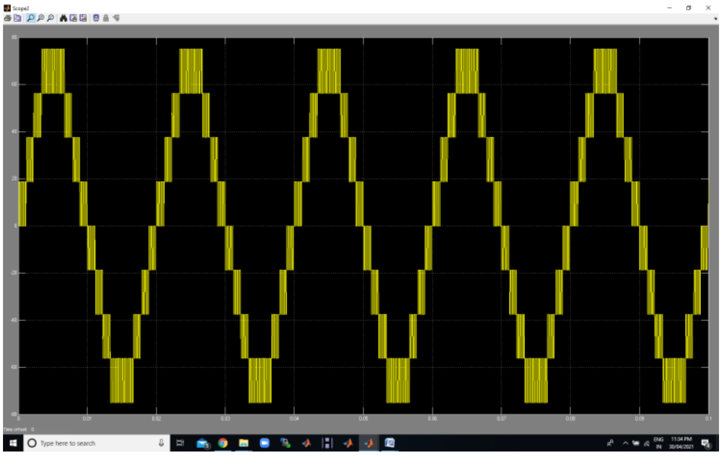
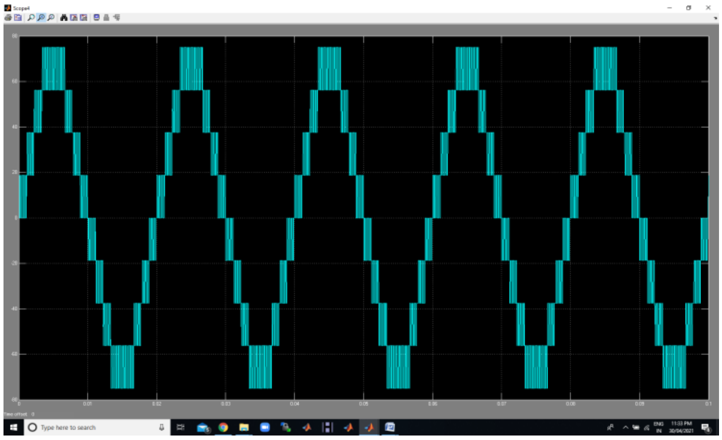
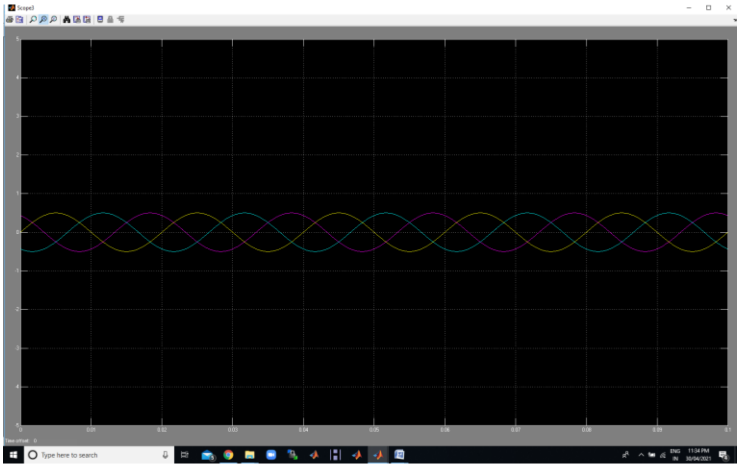
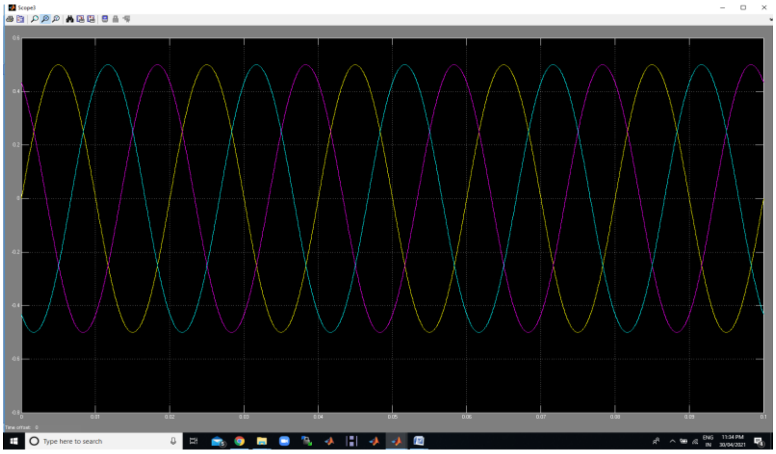


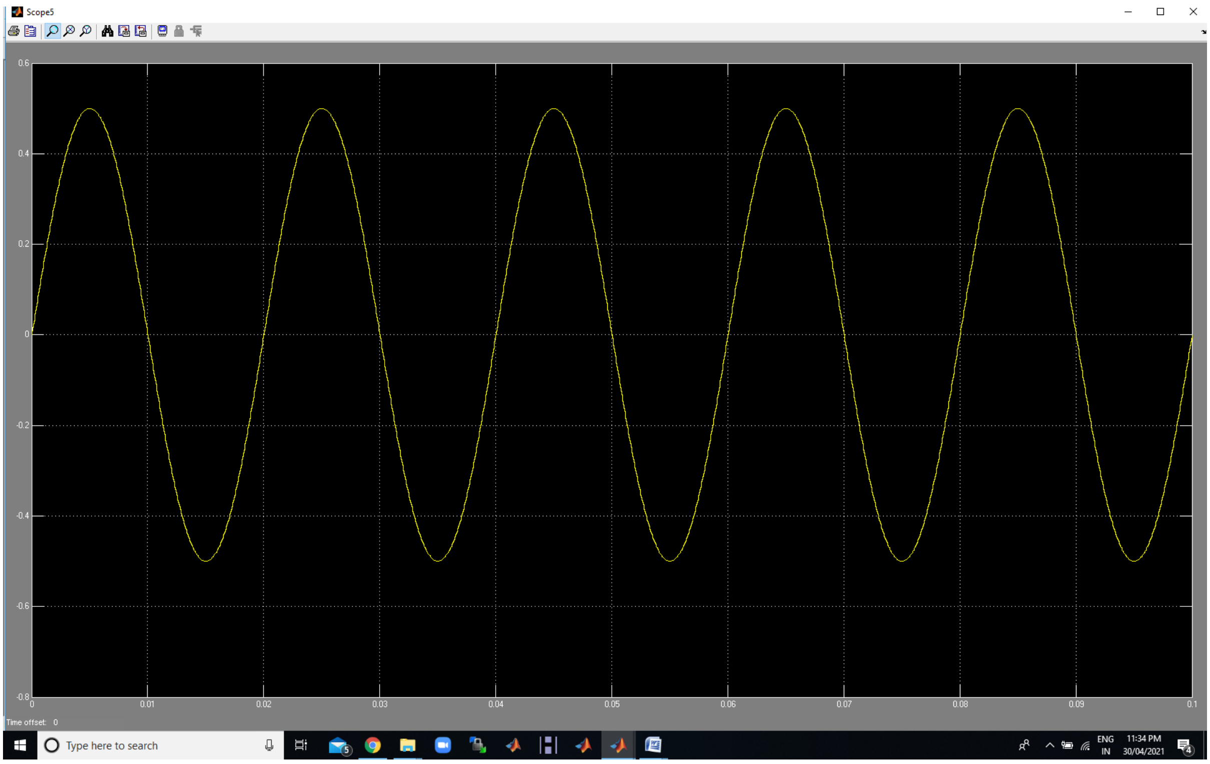
FIGURE 6. Experimental results:(a) V_{inv} & Is at MI = 0.5, ≈1, &> 1, (b) Voltages of different stage V_{inv} , V_{OH} , V_{OL}, Vs, & Is, (c) THD spectra of V_{inv} & Is.







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CONCLUSION

A novel VLB MLI structure introduced in this work along with three different algorithms to choose dc-link magni- tude for producing higher voltage steps using the fewerpart count. Using two RUs with two different varieties of sources, the proposed MLI generates a 15-level output volt- age. In addition to the reduction in the number of switches, both the CLR and TBV are reduced significantly com- pared to the prior-art MLIs. Low CLR value verifies thatthe proposed VLB MLI can easily extend to any numberof levels with a reduced number of components and lower TBV ($16V_{dc}$ for the 15-level MLI) demonstrates suitabil-ity in high-voltage/power applications. The workability of the proposed 15-level MLI is verified in integration withthe 1.3 kW PV system. A closed-loop control strategy is developed, which fulfils all the control objectives, and the system operates satisfactorily for any input or output side perturbations. Simulation and experimental analysis under dynamic test cases such as; different *MI* values, under vary-ing insolation, and grid voltage sag condition validates the satisfactory working of the proposed MLI interfacing PV system. The MPP tracking efficiency of the PV system is about 99.9 %, and the overall system efficiency is morethan 90%.

REFERENCES

Nadipena Ramesh, "Performance Analysis of PI controller fed Reverse Voltage Technique based STATCOM for Power Quality Enhancement", Journal of Green Engineering(JGE)., VOL-10, Issue-10,October 2020, M. di Benedetto, A. Lidozzi, L. Solero, F. Crescimbini, and P. J. Grbovic, ''Five-level E-type inverter for grid-connected applications,'' *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 5536–5548, Sep. 2018.

J. Munoz, P. Gaisse, C. Baier, M. Rivera, R. Gregor, and P. Zanchetta, ''Asymmetric multilevel topology for photovoltaic energy injection to microgrids,'' in *Proc. IEEE 17th Workshop Control Model. Power Electron. (COMPEL),* Jun. 2016, pp. 1–6.

S. K. Chattopadhyay and C. Chakraborty, ''A new asymmetric multi- level inverter topology suitable for solar PV applications with varying irradiance,'' *IEEE Trans. Sustain. Energy*, vol. 8, no. 4, pp. 1496–1506, Oct. 2017.

[1] A. Kumar and V. Verma, ''Performance enhancement of single-phase grid-connected PV system under partial shading using cascaded multilevel converter,'' *IEEE Trans. Ind. Appl.*, vol. 54, no. 3, pp. 2665–2676, May 2018.

C. Cecati, F. Ciancetta, and P. Siano, ''A multilevel inverter for photovoltaic systems with fuzzy logic control,'' *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4115–4125, 2010.

[2] S. Shuvo, E. Hossain, T. Islam, A. Akib, S. Padmanaban, and M. Z. R. Khan, ''Design and hardware implementation considerations of modified multilevel cascaded H-bridge inverter for photovoltaic system,'' *IEEE Access*, vol. 7, pp. 16504–16524, 2019.

[3] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, ''Mod- ular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications,'' *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1722–1731, Mar. 2015.

[4] T. S. Basu and S. Maiti, ''A hybrid modular multilevel converter for solar power integration,'' *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 5166–5177, Sep. 2019.

[5] S. N and U. R. Yaragatti, ''Design and implementation of active neutral-point-clamped nine-level reduced device count inverter: An application to grid integrated renewable energy sources,'' *IET Power Electron.*, vol. 11, no. 1, pp. 82–91, Jan. 2018.

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