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Ultracompact Inverted Input Delay Doherty Power Amplifier with a Novel Power Divider for 5G Mm-Wave

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***Abstract*—This paper reports on the design of a Doherty power amplifier (DPA) for 5G mm-wave applications. Conversely to standard DPAs, this design presents a delay at the input of the carrier amplifier, which enhances the isolation of the peaking amplifier while the DPA is in its low power regime. Moreover, the circuit leverages a novel power divider (PD) to reduce both size and number of passive components. Moreover, the PD transforms the input impedance of the carrier and the peaking amplifiers to 50 Ω avoiding lossy matching networks. Performance consists of a peak gain without pre-driver amplifiers of more than 7 dB at 26.5 GHz, a back-off efficiency plateau of 5 dB, and a saturation power of more than 14 dBm. The circuit has been fabricated in the IHP 130-nm SiGe technology and occupies an effective area of 660x360 μm^2, which makes it suitable to be integrated into a beamformer chip.**

***Index Terms*—5G, Doherty, Power Amplifier, Efficiency, Wilkinson, Divider, Beamformer**

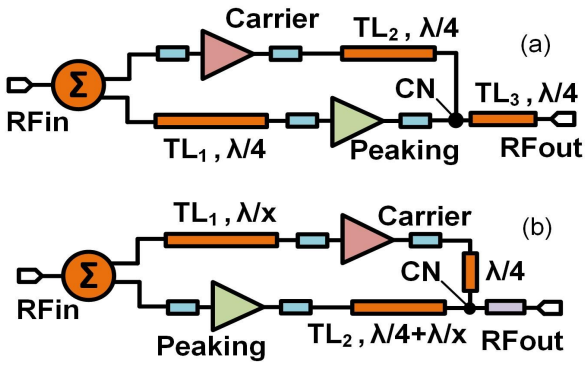

Fig. 1: Block diagram of a (a) standard and (b) proposed Doherty power amplifier.

I. Introduction

The ever-increasing amount of data transmitted with new communication standards dictates stringent requirements regarding the efficiency of the transmitting channel. With the introduction of the fifth-generation mobile communications (5G), the transmitted data using complex modulation schemes have increased. However, employing power amplifiers (PAs) with a high efficiency in the back-off power region is required to counterattack the decreasing efficiency with increasing peak-to-average power ratio (PAPR) [1]. One of the ever-green PAs suitable to increase the power added efficiency (PAE) in the back-off power region and reduce the problems linked to high PAPR signals is the Doherty PA (DPA) [2]. It is known that employing two PAs with a different biasing, namely carrier PA (CPA) and peaking PA (PPA), combined by a $\lambda/4$ transmission line (TL) results in a load modulation that enhances the PAE in the back-off power region. The standard block diagram of a DPA is shown in Fig. 1(a) [3]. Here, the input delay line, TL_1, has been used to compensate the $\lambda/4$ line, TL_2, responsible for the load modulation, and another $\lambda/4$ line, TL_3, has been used to transfer the common-node (CN) impedance to the output impedance. Moreover, phase recovery networks, depicted before and after the PAs, are needed to compensate the phases of the two PAs correctly. Increasing the frequencies, the standard DPA encounters impairments due to the nonidealities of the TLs and the high parasitics of the PAs, which are well described in [4]. However, many works are focusing on enhancing the operating bandwidth [5]–[10] rather than on the load modulation behavior. In this article, the authors propose a technique to reinstate a large and flat back-off PAE, making sure that the PPA is seen as an open circuit at the CN in the low power regime, eliminating the current leakage from the CPA to the PPA leveraging TL_2. The delay, TL_1, at the input of the CPA compensates the delay introduced at the

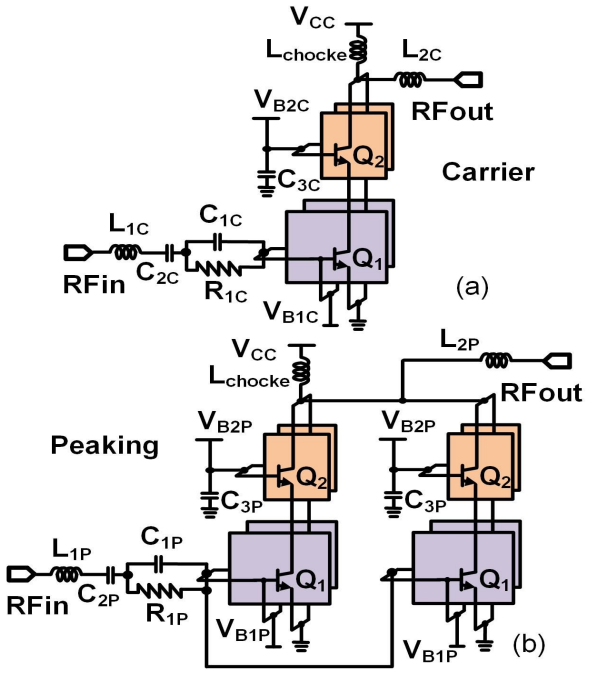

Fig. 2: Schematic of (a) carrier and (b) peaking amplifier.

output of the PPA, as shown in Fig. 1(b). Moreover, artificial transmission lines (ATLs) substitute the TLs since the aim is to cover the $FR2$ $n258$ band (24.25-27.5 GHz) reducing the area occupation. Indeed, a novel power divider (PD) has been used, saving further silicon area and removing part of the lossy input matching network (IMN) [11]. Using lumped components allows for a compact size of the DPA resulting in an occupied area of $660\text{x}360\,\mu\text{m}^2$ making it easily integrable in a beamformer chip. Moreover, the designed DPA shows a PAE back-off region of $5\,\text{dB}$.

II. Circuit Architecture

A highlight of the architecture has been provided in the previous subsection and in the block diagram of Fig. 1(b). In this section, further details and design choices are given.

A. Carrier and peaking amplifiers

In Fig. 2, the schematic of both CPA and PPA are depicted. The designed DPA has an asymmetrical topology, and therefore the PPA, in Fig. 2(b), has double the number of the heterojunction bipolar transistors (HBTs) with respect to the CPA. Both PAs are based on a cascode topology sharing the same supply, V_{cc}, of $3.3\,\text{V}$ fed by chocke inductors, L_{chocke}, as shown in Fig. 2. The common-base amplifier (CB) biasing voltage is the same for both amplifiers, while the biasing voltage of the common-emitter amplifiers (CE) differs. Indeed, the CPA is biased in deep class AB, while the PPA is biased in class C. The HBTs of the CB and the CE have eight fingers each for both CPA and PPA. Load-pull simulations help to select the output inductors, $L_{2\text{C}}$ and $L_{2\text{P}}$, chosen to maximize efficiency by resonating out the parasitic capacitance

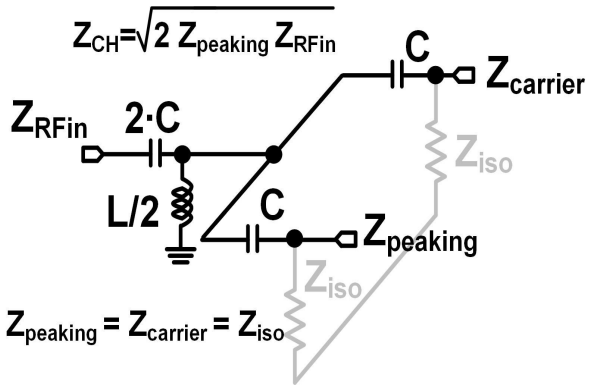

Fig. 3: Schematic of the proposed power divider.

at the output of the CPA and PPA, respectively. At the input of the CEs, a stabilization network made of a capacitor, C_1, and a resistor, R_1, is added. Moreover, source-pull simulations are performed along with the insertion of the series inductors, $L_{1\text{C}}$ and $L_{1\text{P}}$, to resonate out the input capacitive part of the CEs and resulting in the same input impedance for both CPA and PPA. Using this technique, the PPA can be directly attached to the PD, and the input of the CPA is fed by the signal coming from the ATL after the PD, namely TL_1 in Fig. 1.

B. Third harmonic filter

At the output of the PPA and the CPA, a parallel inductor/capacitor filter has been placed to increase the PAE of both PAs. The filter, not shown in Fig. 2 for simplicity, consists of a $60\,\text{fF}$ capacitance and a $70\,\text{pH}$ inductor, resonating at around $78\,\text{GHz}$. The third harmonic is bounced back to the cascode generating a voltage wave similar to class-F amplifiers, hence, enhancing the efficiency.

C. Power divider

For saving area, the power divider from [11] is used. This PD is directly matched to two impedances. Indeed, at the input terminal the impedance, Z_{RFin}, in Fig. 3 is $50\,\Omega$, while the impedance seen towards the two PAs is the resistive part of the PPA input impedance, Z_{peaking}, which is the same of the CPA, $Z_{\text{carrier}} = Z_{\text{peaking}}$. The occupied silicon area by the designed PD is only $56\text{x}90\,\mu\text{m}^2$, in agreement with the size presented in [11]. The ATLs of the PD have a characteristic impedance, Z_{CH}, which is based on

$$Z_{\text{CH}} = \sqrt{2 Z_{\text{peaking}} Z_{\text{RFin}}}\,. \tag{1}$$

Moreover, the resistance of the isolation network, Z_{iso}, is given by

$$Z_{\text{iso}} = \frac{Z^2{}_{\text{CH}}}{2 Z_{\text{RFin}}} = Z_{\text{peaking}}. \tag{2}$$

It is straightforwad to conclude that $Z_{\text{carrier}} = Z_{\text{peaking}} = Z_{\text{iso}}$. The PD of Fig. 3 is based on two high-pass ATLs whose inductors are then combined [11]. To calculate the value of each lumped component,

$$C = \frac{1}{\omega Z_{\text{CH}}}\,,\; L = \frac{Z_{\text{CH}}}{\omega} \tag{3}$$

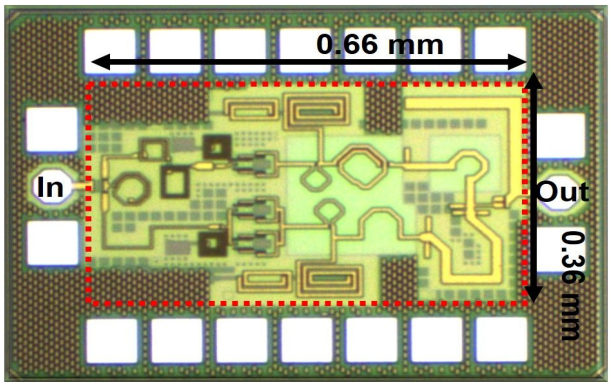

Fig. 4: Micrograph of the fabricated Doherty power amplifier.

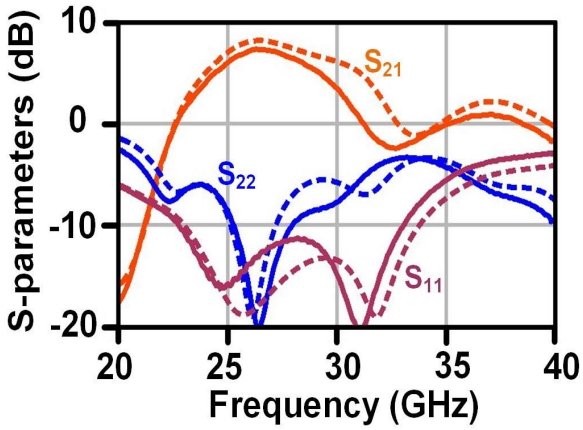

Fig. 5: Simulated (dashed line) and measured (straigth line) S-parameters.

must be used. Inserting (1) in (3), the numerical value for C and L is calculated, and then L is divided by two for calculating the inductance and C at the input is multiplied by two, as shown in Fig. 3.

D. Artificial transmission lines

As mentioned above, the TLs have been substituted by lumped counterparts by means of ATLs and the values of their components have been chosen in order to avoid current leakage to the PPA during low power operations. In Fig. 1(b), TL_1 and TL_2 are not $\lambda/4$. The CN impedance is chosen according to [8] and TL_2 is given by

$$TL_2 = \lambda/4 + \lambda/x \tag{4}$$

where λ/x is the electrical length needed to show an open circuit at the CN when the PPA is off. However, when the PPA turns on, TL_2 matches the PPA to the CN. TL_1 is the residual electrical lenght λ/x. The $\lambda/4$ removal at the PPA input with the addition of TL_2 at its output makes a delay of the PPA at the CN which is then compensated by the insertion of TL_1.

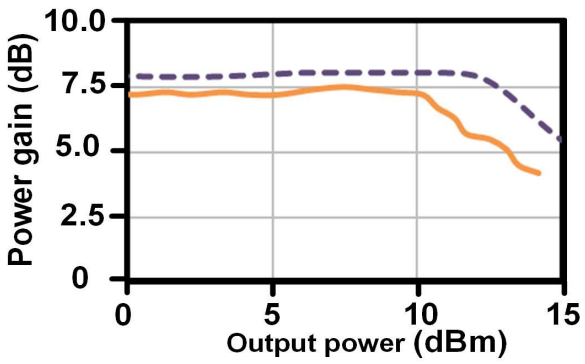

Fig. 6: Simulated (dashed line) and measured (straigth line) power gain across output power at a frequency of 26.5 GHz.

III. Measurement Results

The designed DPA is shown in Fig. 4 and it occupies a silicon area of $660\times360\,\mu\text{m}^2$. The chip has been fabricated using the IHP SG13S SiGe technology which leverages an $f_t/f_{\max}$ of 250/340 GHz. Moreover, the technology comprehends a back-end-of-line (BEOL) of seven metal layers with two top thick ones. Indeed, passive components such as inductors and TLs are designed using those top metals, while the technology also provides metal-insulator-metal (MIM) capacitors. The DPA has been characterized on-wafer using a ZVA67 from R&S® for the S-parameters, while continuous wave (CW) measurements have been performed using a SM R600 signal generator and a NRP-Z57 power meter. Fig. 5 shows the S-parameter measurements. The transmission parameter, S_{21}, shows a match between simulations and measurements with a difference of only 0.7 dB in the band of interest, and its peak is 7.3 dB. Return loss measurements show a small deviation from simulations. Nevertheless, the measured S_{11} is lower than -10 dB in the targeted band. The results of CW measurements are reported in Fig. 6 and Fig. 7. Fig. 6 shows the simulated and measured power gain versus output power. The power gain is 7.3 dB in the low power region and then the nonlinearity of the DPA slightly increases it. The output 1-dB compression point ($\text{OP}_{1\text{dB}}$) is 11.3 dBm, whereas the saturated power cannot be correctly estimated due to the saturation of the measurement setup. However, the maximum measured output power is 14.5 dBm. Collector efficiency (η) and PAE are plotted in Fig. 7. Here, PAE reaches a peak of 14.3%, while remaining over 12.5% for a back-off of 5 dB.

IV. Conclusion

This paper explores a topology of Doherty PA that avoids the leakage of current from the carrier amplifier to the peaking amplifier. This is done inverting the delay between the carrier and the peaking. Moreover, a novel power divider has been introduced. The design is based on lumped components making it suitable for the integration in beamformer chips. The area occupation is only $660\times360\,\mu\text{m}^2$. A peak gain of 7.3 dB, $\text{OP}_{1\text{dB}}$ of 11.3 dBm and a region of 5 dB PAE back-off.

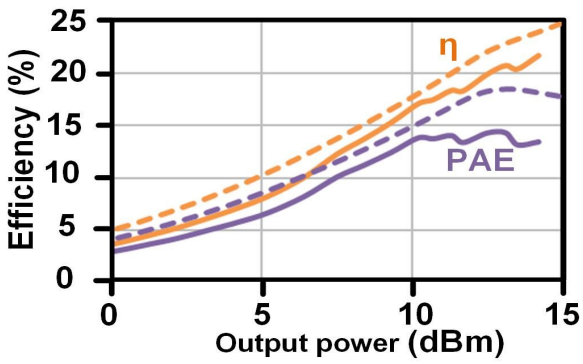

Fig. 7: Simulated (dashed line) and measured (straigth line) efficiency across output power at a frequency of 26.5 GHz.

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REFERENCES

[1] F. Sandoval, G. Poitau, and F. Gagnon, "Hybrid Peak-to-Average Power Ratio Reduction Techniques: Review and Performance Comparison," *IEEE Access*, vol. 5, pp. 27 145–27 161, 2017.

[2] P. Colantonio, F. Giannini, R. Giofrè, and L. Piazzon, "The AB-C Doherty power amplifier. Part I: Theory," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 19, no. 3, pp. 293–306, 2009. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/mmce.20350

[3] A. Grebennikov and S. Bulja, "High-efficiency doherty power amplifiers: Historical aspect and modern trends," *Proceedings of the IEEE*, vol. 100, no. 12, pp. 3190–3219, 2012.

[4] P. M. Asbeck, "Will Doherty continue to rule for 5G?" in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, 2016, pp. 1–4.

[5] P. Indirayanti and P. Reynaert, "A 32 GHz 20 dBm-PSAT transformer-based Doherty power amplifier for multi-Gb/s 5G applications in 28 nm bulk CMOS," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2017, pp. 45–48.

[6] S. Hu, F. Wang, and H. Wang, "A 28-/37-/39-GHz Linear Doherty Power Amplifier in Silicon for 5G Applications," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 6, pp. 1586–1599, June 2019.

[7] N. Rostomyan, M. Özen, and P. Asbeck, "28 GHz Doherty Power Amplifier in CMOS SOI With 28% Back-Off PAE," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 5, pp. 446–448, May 2018.

[8] X. A. Nghiem, J. Guan, and R. Negra, "Broadband sequential power amplifier with doherty-type active load modulation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 9, pp. 2821–2832, 2015.

[9] K. Choi, H.-J. Yoo, J. Ha, J. Kim, J. Kim, B. Jo, S. Kim, J. Park, Y. Na, and Y. Hur, "A 5g mm-wave single chip 8-channel fem with best-in-class 22% power efficiency and embedded die substrate (eds) technology," in *2021 IEEE MTT-S International Microwave Symposium (IMS)*, 2021, pp. 721–724.

[10] D. Wang, W. Chen, X. Chen, X. Liu, F. M. Ghannouchi, and Z. Feng, "A 24-29.5 ghz voltage-combined doherty power amplifier based on compact low-loss combiner," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 7, pp. 2342–2346, 2021.

[11] A. Franzese, R. Negra, and A. Malignaggi, "An n-way single-inductor high-pass power divider for 5g applications," *IEEE Solid-State Circuits Letters*, vol. 5, pp. 5–8, 2022.